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7590 05/01/2002

MATTINGLY, STANGER & MALUR, P.C.  
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APPLICATION NO. 09/922,656	FILING DATE 08/07/2001	FIRST NAMED INVENTOR Yoshihiko Okamoto	ATTORNEY DOCKET NO.	CONFIRMATION N. 9695
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TITLE OF INVENTION: PROCESS FOR FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND EXPOSING SYSTEM AND MASK  
INSPECTING METHOD TO BE USED IN THE PROCESS

APPLN. TYPE nonprovisional	SMALL ENTITY NO	ISSUE FEE \$1280	PUBLICATION FEE \$300	TOTAL FEE(S) DUE \$1580	DATE DUE 08/01/2002
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EXAMINER BARRECA, NICOLE M	ART UNIT 1756	CLASS-SUBCLASS 430-311000
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(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Hitachi, Ltd.

Tokyo, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ individual ☒ corporation or other private group entity ☐ government

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